REMARKS

The Office Action of September 21, 2007 was received and carefully reviewed. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

By this amendment, claims 1, 21 and 26 are amended. Consequently, claims 1-29 are currently pending in the instant application, of which, claims 6-20 being withdrawn from further consideration by the Examiner as being directed to a non-elected invention.

Claims 1, 3-5, 21, 23-26, 28 and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art (APA) in view of Rozman (U.S. Patent No. 5,177,745), McGibney et al. (U.S. Patent No. 6,112,322), and McClure (U.S. Patent No. 6,037,792). Claims 2, 22 and 27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over admitted prior art in view of Rozman, McGibney et al., McClure, and further in view of Fontana et al. (U.S. Patent No. 5.982.677). APA, Rozman, McGibney et al., McClure, and Fontana et al., however, fail to render the claimed invention unpatentable. Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. For example, independent claim 1 recites a combination that includes, among other things:

> a test mode circuit for outputting a test mode signal according to a predetermined voltage to a predetermined terminal of the plurality of address input terminals when a signal is inputted to the predetermined terminal among the address input terminals, said test mode circuit operatively connected to inhibit the voltage to a selected memory cell via the test mode signal.

Independent claim 21 recites yet another combination that includes, *inter alia*,

> a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal according to a predetermined voltage to a predetermined terminal of the plurality of address input terminals in response to the address signals received thereto, said test mode circuit operatively connected to inhibit the voltage to a selected memory cell via the

test mode signal.

Independent claim 26 recites a further combination that includes, for instance,

> a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal according to a predetermined voltage to a predetermined terminal of the plurality of address input terminals in response to the address signals received thereto, said test mode circuit operatively connected to inhibit the voltage to a selected memory cell via the test mode signal.

At the very least, the applied references, whether taken alone or in combination, fail to disclose or suggest any of these exemplary features recited in independent claims 1, 21 and 26.

In accordance with the present invention, in a nonvolatile semiconductor memory device (e.g., see Figs. 1-4), each of the memory devices of the disclosed embodiments has a plurality of memory cells including a first electrode, second electrode and gate electrode. The first electrode may receive an applied voltage such as that generated by a regulator. The second electrode is connected to a corresponding one of bit lines, and the gate electrode is connected to a corresponding one of bit lines. Furthermore, the gate electrode is connected to a corresponding one of word lines. The nonvolatile semiconductor memory device, according to the present invention, may further include a test mode circuit. The test mode circuit may perform to inhibit an applied voltage from the regulator to the first electrode by the test mode signal. The test mode signal is outputted outside using a monitor terminal or one of an output terminals. Accordingly, each of the disclosed nonvolatile semiconductor memory devices is able to confirm a test state by monitoring the voltage of the test mode signal which is used to control the application of voltage to a first electrode on the monitor terminal or one of output terminals.

Turning to the prior art, none of the prior art references, whether taken alone or in combination, disclose or suggest each and every feature recited in the claims. In particular,

for example, APA fails to disclose a test mode circuit operatively connected to inhibit the voltage to a selected memory cell via the test mode as recited in claims 1, 21, and 26. Rozman, McGibney et al., McClure, and Fontana et al., fail to cure the deficiencies of APA.

In accordance with the M.P.E.P. § 2143.03, to establish a *prima facie* case of obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 409 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 196 (CCPA 1970). Therefore, it is respectfully submitted that neither APA, Rozman, McGibney et al., McClure, nor Fontana et al., taken alone or in any proper combination, disclose or suggest the subject matter as recited in claims 1, 21 and 26. Hence, withdrawal of the rejection is respectfully requested.

Each of the dependent claims depend from one of independent claims 1, 21 or 26 and are patentable over the cited prior art for at least the same reasons as set forth above with respect to claims 1, 21 and 26.

In addition, each of the dependent claims also recite combinations that are separately patentable.

In view of the foregoing remarks, this claimed invention, as amended, is not rendered obvious in view of the prior art references cited against this application. Applicant therefore request the entry of this response, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

In discussing the specification, claims, and drawings in this response, it is to be understood that Applicant in no way intends to limit the scope of the claims to any exemplary embodiments described in the specification and/or shown in the drawings. Rather, Applicant is entitled to have the claims interpreted broadly, to the maximum extent permitted by statue,

regulation, and applicable case law.

Should the Examiner believe that a telephone conference would expedite issuance of the application, the Examiner is respectfully invited to telephone the undersigned patent agent at (202) 585-8316.

Respectfully submitted,

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